LOW POWER TECHNIQUES FOR LEAKAGE POWER MINIMIZATION

Borisav Jovanović, Milunka Damnjanović, *Faculty of Electronic Engineering Niš*

Abstract – *Low-power design techniques for leakage power minimization are investigated and presented in this paper. Emphasis is on modern standard cell process technologies, and also, modifications in IC design tools. Presented low-power techniques are applied on 8051 microcontroller block which is embedded in Integrated Power Meter System-On-Chip.*

1. INTRODUCTION

Power dissipation is today one of the key parts of design specifications of the System-on-Chip (SoCs), complex analog and digital systems integrated on the single IC. Also, power consumption is competitive differentiator of many ICs in today's electronic industry. ICs incorporated into wireless, portable or home entertainment devices must minimize their power consumption for cost and energy efficiency reasons.

As technology process is scaled down to nanometer range, the importance of leakage power minimization is exponentially increasing. In SoCs implemented in modern technologies, the amount of leakage power can represent significant part (even a half) of total power.

In the design of low power SoC devices, it is often necessary to conduct power optimization as early as possible. Any decision made at the architectural level would have significant impact on power minimization results. This stands also for leakage power minimization. It is important to consider leakage minimization at the beginning of chip design, although leakage reduction must be included in the next steps of standard IC design flow, in synthesis and place and route process.

In this paper, low power design techniques which have an emphasis on modern standard cell process technologies are presented and investigated. Special attention is put on leakage power minimization. As an example, 8051 microcontroller block is used, which is embedded into Integrated Power Meter IC. The crucial parts of microcontroller design flow, that are presented in the paper, are related to leakage power estimation and minimization. The leakage minimization is especially important in microcontroller power down modes which do not have intensive data processing.

2. POWER CONSUMPTION SOURCES

The major sources of power dissipation in digital CMOS circuits can be divided into dynamic ($P_{dynamic}$) and the leakage power ($P_{leakage}$), summarized by following power equation:

$$P_{average} = P_{dynamic} + P_{leakage} \quad (1)$$

Dynamic power is composed of internal power and switching power:

$$P_{dynamic} = P_{internal} + P_{switching} \quad (2)$$

Internal power includes short-circuit (VDD to ground) and power consumption in switching of standard cell internal nets.

$$P_{internal} = V_{DD} I_{SC} + P_{int\text{-}switching} \quad (3)$$

Switching power which contributes most of the dynamic power consumption is due to charging and discharging of load capacitance during switching:

$$P_{switching} = \alpha C_L V_{DD}^2 f_{CLK} \quad (4)$$

where α is the switching activity factor, C_L the total node capacitances of the circuit, V_{DD} the power supply voltage and f_{CLK} is the clock frequency. Dynamic power in designs is growing rapidly because of increase in chip's clock frequencies and chip's size. Lowering the dynamic consumption implies reducing some of these factors and can be applied at several levels of abstraction: technology, circuit, gate, architecture and system levels.

Leakage power [1] is mainly due to sub-threshold currents from gate oxide leakage when transistor is off.

$$\begin{aligned} P_{leakage} &= V_{DD} \cdot I_{leakage} \\ &= V_{DD} \cdot I_0 \exp\left((V_{GS} - V_{TH}) / nV_T\right)\left(1 - \exp(-V_{DS} / V_T)\right) \end{aligned} \quad (5)$$

where V_{TH} is the threshold voltage of the transistor, V_T is thermal voltage (equal to 26mV at 25°C), V_{GS} is voltage between gate and source, and V_{DS} is voltage between drain and source.

Since sub-threshold current is exponentially proportional to the negative value of threshold voltage ($-V_{TH}$), leakage power consumption increases exponentially with decreasing V_{TH} (equation (5)). As transistor size is scaled down in new technologies to nanometer range, the influence of leakage power on total power dissipation is rapidly increasing. In the 350nm technology the leakage currents were insignificant comparing to dynamic currents. In the newer CMOS technologies, starting from 90nm and below, leakage power consumption form significant part of the total power consumption. The exponential relation between leakage power and technology scaling is given in Fig.1.

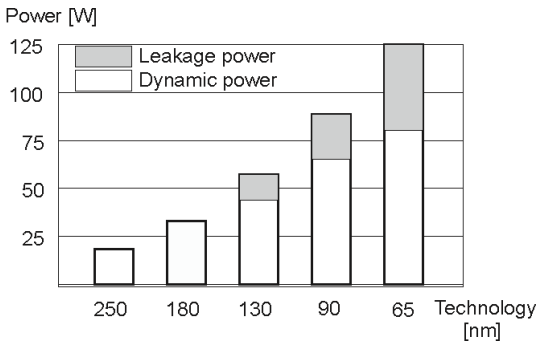

Figure 1. *Impact of technology scaling on leakage power share in the total power for SoC design*

3. LEAKAGE POWER MINIMIZATION

As technologies are moving towards nanometer range, accurate leakage power estimation and efficient leakage power optimization become crucial for any low power

solution. The following leakage elimination techniques are used today: voltage scaling, multi voltage design, multi threshold standard cell libraries and power gating. Next, the techniques are explained and their application on 8051 microcontroller design is described..

Reducing the supply voltage

The first technique used for decreasing the leakage consumption is to reduce power supply. The leakage power reduces linearly with the decreasing of supply voltage Vdd (this can be concluded from leakage power equation (5)). Reducing the supply voltage is particularly useful in power saving modes of SoCs when no fast and intensive data processing is required. For example, when SoC is in the power saving mode, the memories incorporated into SoC can be supplied by lower voltage than voltage used in the active operation mode. The lower voltage used in the power save mode preserves the RAM content.

Multiple threshold voltage cells

Multiple threshold voltage libraries offered by standard cell technologies are essential in leakage optimization. The digital logic cells are present usually in two forms:

- High V_{TH} cell library have lower leakage currents and therefore consume less power but have larger delays. They are slow cells.

- Low V_{TH} cells have the good timing characteristics but consume more power then high V_{TH}.

Synthesis tools have to perform very complicated optimization and to use high V_{TH} cells in the design as much as possible for leakage power minimization. In those parts of circuit where timing requirements are critical, faster cells that have low V_{TH} have to be used by synthesis tools. There is a huge difference in leakage power consumption despite small difference in delay between cells from different V_{TH} libraries [1].

Power shutdown

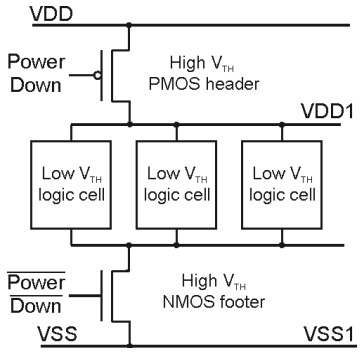

Figure 2. *MTCMOS switches for power shutdown*

A far more aggressive and effective technique for leakage decreasing is to simply cut the power supply to any inactive transistor. Usually, entire design blocks are put in the shutdown state.

Power gating is done by placing one PMOS transistor and one NMOS transistor in series with the transistors of each block to create virtual ground and virtual power supply (VDD1 and VSS1 in fig..2). Switches in the power network are called MTCMOS header switches, and MTCMOS footer switches in the ground network. Because of lower on resistance, header switches are usually used [3].

Isolation cells

In multi voltage designs, when design block is switched off, it is important to ensure that output signals of shutdown block that drive active area will not be left floating. Isolation cells are special type of cells that are inserted at voltage area boundaries that prevent propagation of undesired signals. They preserve CMOS logic levels on the power gated outputs (Fig.3).

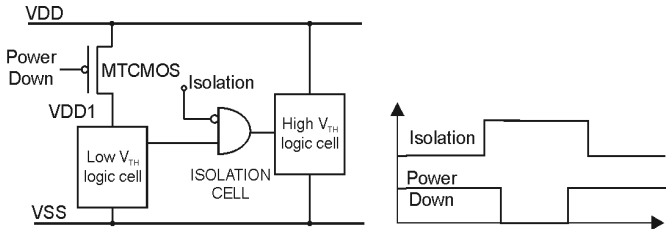

Figure 3. *Isolation cell and relevant signals*

State retention cells

Since power gating technique switches on and off circuits from power supply and ground nets, it also disconnects latches and flip-flops, which results in loss of their contents during shutdown. One solution to this problem is, for example, using application software for writing data in nonvolatile memories (or memories which have steady power supply) and using scan chains to shift in data into memories before starting shutdown. After power up sequence is finished, data is shifted out from memories into sequential elements. This method can be very slow in real case applications and is often not acceptable for the most SoC applications.

More advanced solution is using State Retention Power Gating (SRPG) Flip Flops in order to efficiently preserve state (Fig. 4).

The SRPG cell has main power supply input (VDD in Fig) for active operation when it can change its state. Beside, cell introduces an extra power supply input, called retention voltage (VRET in Fig) for state retention purpose. When main supply VDD is switched off, VRET is enough to save the state. The relevant signal sequence is given in fig.. 4. Signal RET puts the SPRG cell in state preserving state. While RET is active, power supply net VDD can be disconnected (signal Pwr is 0).

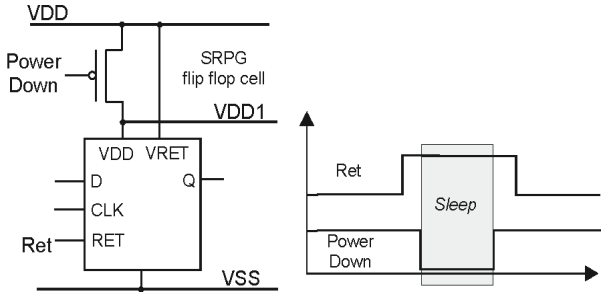

Figure 4. *State retention flip-flop cell and relevant signals*

Power gating method which uses one MTCMOS transistor for each logic gate is known as Fine Grain Power

Switch. It results in large area and power overhead.

Another type of switches supported by modern technologies, which switches a group of gates, is called Course Grained Power Switch.

In Course Grained Power Switch, power switch can contain a number of segments. Each segment can contain one or more transistors which share drain, gate and source. The power switch segments can be arranged in ring style or grid style.

Ring style shown in Fig.5 has advantage in minor influence in place & route design flow and it is the only solution when incorporating hard IP digital blocks. The disadvantages are in the fact that isolation cells and always-on buffers are placed outside the block. Also, ring style does not support the retention registers and the IR drop could be large for big blocks.

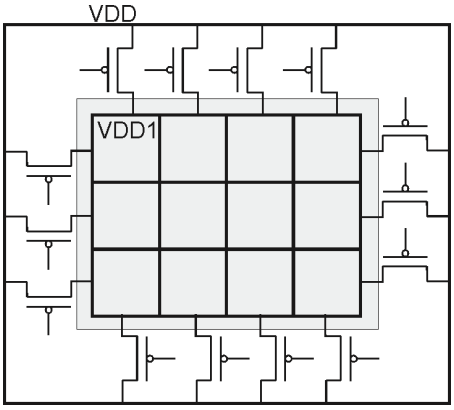

Figure 5. *Ring style Course Grained Power Switch*

Grid style Course Grained Power Switch is given in Fig. 6. It has advantage in better IR drop management and better optimized sleep transistor distribution. It occupies less area and supports isolation cells, always-on buffers and retention cells. Only disadvantage is that it is not always possible for implementation in hard IP blocks

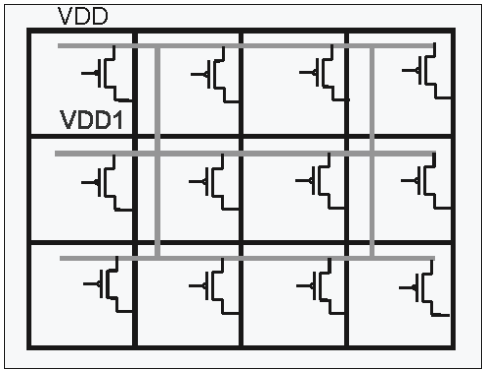

Figure 6. *Grid style Course Grained Power Switch*

4. LEAKAGE POWER MINIMIZATION APPLIED ON 8051 MICROCONTROLLER BLOCK

The chip was implemented in two technologies: AMIS CMOS 350nm and Synopsys 90nm.

The power supply voltage is 3.3V for AMIS 350nm and 1.2V for Synopsys 90nm technology. For the implementation in Synopys 90nm technology, Synopsys IC development tools are used: Design Compiler for synthesis and IC Compiler for floorplannig, placement and routing. The AMIS 350nm technology is provided with a support in Cadence tools: RTL Compiler for synthesis and SoC Encounter for layout implementation.

The information about static and dynamic power consumption of digital standard cells is provided by technology files. The power consumption of microcontroller core is obtained after layout implementation, and detail, Verilog netlist logical verification while which the total switching activity of core's nets was recorded. The power consumption is determined in Prime Time Synopsis tool for 90nm Synopsys implementation, and by SoC Encounter Cadence tool for 350nm implementation.

In 350nm technoligy, the leakage currents were insignificant comparing to dynamic currents. The reduction of clock frequency and utilization of clock gating techniques were successful in eliminating the power consumption for more than 50%. Total dissipation of microcontroller core in 350nm technology was 3.5mW.

Change of chip technology from 350nm to 90nm showed the clear necessity for leakage power reduction. In 90nm technology, in microcontroller applications which don't require high clock frequencies, the leakage power becomes dominant part of total power consumption.

The power consumption of MCU in 90nm was measured to be 0.68mW at the chip frequency of 3.75MHz. The leakage power of 0.41mW forms almost 60% of total power. The dynamic power of power optimized design is only 0.27mW.

The following leakage minimization techniques were implemented in MCU core: supply voltage reduction, utilization of multi-V_{TH} libraries and power gating. The techniques rely on the additional support in synthesis and implantation phases, including new methods in floorplanning, placement, clock tree generation and routing phases.

The RTL description of MCU had to be modified significantly to make the leakage reduction possible. The design had to be partitioned into three voltage domains: MCU core, the peripherals and memories. Each voltage domain has its own power supply net which is derived from the main net Vdd. The utilized technology Synopsys 90nm provides only header MTCMOS transistors which were used in grid style course grained power switch network. The supply VDDCORE was used to supply the microcontroller core. Net VDDPER is chosen for peripheral's supply. The memories (two 4kB RAM for program storing, two 1kB XRAM, two 128B Dual Port IRAM blocks) use the VDDMEM supply line while the Power management unit is supplied by main supply net - VDD.

As it was stated previously, the microcontroller core, beside Active operation mode, offers two power saving modes: Standby and Power Down.

In Standby mode, the microcontroller's core is switched off from power supply while the peripherals and memories were kept powered. Power management unit turns off the VDDCORE while keeping the VDDPER and VDDMEM. The memories are powered to retain the program code and data. The peripherals (including three parallel data

input/output ports, three timer/counter modules and two USART modules) are kept powered to enable the wake up sequence and MCU safe returning into Active mode.

In Power Down mode both the MCU core and peripheral units are powered down. All three voltage domain's supply nets are switched off. In Power Down only the chip reset signal can return the microcontroller from Power Down to the Active mode.

The functioning of Power management unit in the Standby mode includes following operations. Before entering the Standby, when are in Active mode, the peripherals are managed through Special Function Registers. The changes in architecture are related to location on specific SFR registers. The peripheral's control registers had to be physically implemented in peripheral's voltage domain. Also, the SFR registers which control the interrupts are made to be part of peripheral's voltage area. These changes ensure that switching off the microcontroller core's power doesn't have influence on peripheral's operation and on interrupt detection. The peripherals simply continue to function when microcontroller changes the mode from Active to Standby.

The Standby mode is started by writing the sequence "10" into two least significant bits of PMSR register. The PMSR is one of SFRs and is physically implemented in the Power management unit.

While bringing the chip into the Standby mode, the Power management unit performs several operations. First, it issues the reset signal for MCU core. Then, it activates the isolation cells located on the interface between MCU core and the neighboring blocks, including peripheral block and memories. These blocks have to be under power supply during the Standby. At the end of Standby beginning sequence, the Power management unit activates the Sleep signal to activate MTCMOS cells. The Sleep signal switches off the MCU core from VDD.

The power supply of microcontroller's core, VDDCOR, is in the off state until peripheral interrupt occurs. When it occurs, the Power management block receives the information from interrupt control logic (part of peripheral voltage area) and starts the power restoring procedure. The power restore does not happen suddenly. Instead, it consists of several phases. First, Sleep signal controlling the MTCMOS cells is put into reset state which starts the raising of the power supply VDDCOR. After time period long enough for power supply restoring, the control signal for isolation cells is asserted. At the end of returning into Active mode, the MCU core is removed from the reset state. Then, the microcontroller's core begins the program code execution and immediately enters into the software routine for the interrupt which caused the transition from Standby to Active mode.

It is important to keep in mind that when chip is in Standby, the relevant data is retained in RAM memory blocks (which remain powered) and all cells in microcontroller's core are switched off. Therefore, there was no need for retention sequential cells.

The power gates (header switches) were laid out as double height cells in columns. The cells pin connectivity is done by abutment in the placement area where the synthesized core cells are placed. To manage them in rush current during power-up starting as well as to reduce the IR drop, the switch network was implemented as a daisy chain of power gates.

The power reduction achieved in Standby mode is 75% comparing to the design which did not use the benefits of power gating in 90nm technology. The leakage power became 0.1mW instead of 0.4mW that was before use of the leakage reduction techniques.

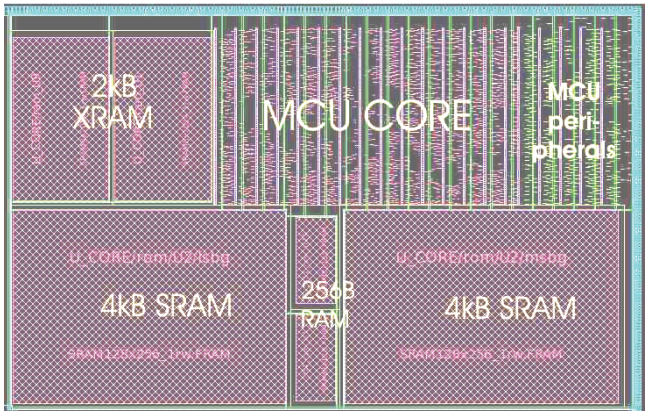

Figure 7. *The MCU layout in 90nm technology*

5. CONCLUSION

In this paper, a leakage low power techniques are presented and applied on microcontroller design. The considered technology is Synopsis 90nm.

The leakage minimization techniques implemented in MCU core are: supply voltage reduction, utilization of multi-V_{TH} libraries and power gating. The leakage power reduction in 90nm technology achieved by power saving modes is 75%.

The main objective, which was to realize power efficient design, was fully reached. Measurements on the chip, which will be manufactured, have to be carried out to confirm those results.

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